49. The ATM switch according to claim 42, wherein the data buffers are physically associated with input ports.

50. The ATM switch according to claim 42, wherein the data buffers are physically associated with output ports.

51. The ATM switch according to claim 42, wherein the rate limitation is enforced at inputs.

52. The ATM switch according to claim 42, wherein the rate limitation is enforced at outputs.

53. The ATM switch according to claim 42, wherein each of the data units designates a priority and an input port and the determination of whether the additional data units which designate relatively low priorities and a particular input port are in violation of the rate limitation is based on a "leaky bucket" algorithm.

54. The ATM switch according to claim 53, wherein the particular input port is associated with a selected store whose backlog caused the selective filtering condition to be imposed.

REMARKS

Claims 1-5, 7-16 and 18-54 are currently pending in this application. Claims 1, 10, 33 and 42 have been amended. Applicant respectfully submits that the claims currently pending in this case are patentably distinguishable over the cited references, and reconsideration and allowance are respectfully requested.

In an Office Action date August 10, 2001, the Examiner objected to the drawings under 37 C.F.R 1.83(a) for allegedly failing to show output controls arranged to monitor the backlog of data units buffered in two or more of the plurality of data stores for delivery to their

associated output ports. Applicant has submitted herewith an amended FIG. 3 such that data buffer 340 comprises a plurality of operatively distinct data stores e.g. (Data $Store_1$ through Data $Store_P$). The proposed changes are shown in red in the amended drawing. The proposed changes are supported by the originally filed specification which teaches that data buffer 340 in FIG. 3 "has operatively distinct stores for buffering data units according to their particular characteristic, such as priority. For a switch supporting P levels of priority, data buffer 340 preferably has P stores for separately buffering data units for each particular priority". (page 8, lines 2-3). Applicant therefore respectfully submits that no new matter has been added and requests that the amended drawing be entered and the objection withdrawn.

The Examiner rejected claims 1, 5, 7-10, 16, 18-20, and 22 under 35 U.S.C. 102(e) as allegedly being anticipated by Ramamurthy et al (U.S. Pat. No. 6,046,901). Applicant respectfully traverses this rejection.

Independent claims 1 and 10 recite an ATM switch wherein each of a plurality of output ports are (paraphrasing) "operatively associated with a plurality of output data stores and an output control... wherein the output data stores <u>on an output side of the switch fabric</u> are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to monitor the backlog of buffered data units <u>in one or more of said plurality of output data stores</u> for delivery to their associated output ports ..." The cited reference does not disclose or suggest a switch having a plurality of output ports, wherein each of the output ports is operatively associated with a plurality of output data stores on the output side of the switch and output controls arranged to monitor the backlog of buffered data units stored in one or more of the output data stores.

Rather, referring to FIG. 9 and col. 22 lines 42-52, Ramamurthy discloses an ATM switch having two input ports (910, 920) with traffic streams directed to certain output port(s). Each input port is associated with two input buffers, one for CBR (915,925) connections and another for VBR (917,927) connections on the input side of the switch fabric. Further in the system taught by Ramamurthy each output port is operatively associated with only a single output buffer that serves the two input ports in a work-conserving, round-robin manner. In this system a back pressure signal 930 is sent back to stop cell transmission when the output buffer is full.

Thus in Ramamurthy the output control is only associated with a single data store on the output side of the switch. Further the output control of Ramamurthy simply monitors the level of the single output data store and stops transmission when the buffer is full. Ramamurthy does not therefore monitor the backlog of buffered data units stored in one or more of a plurality of output data stores on the output side of the switch.

Therefore, applicant respectfully submits that claims 1 and 10 each recite a novel and unobvious apparatus in view of Ramamurthy and should therefore be allowed. Further claims 2-5, and 7- 9 and claims 11-16 and 18-22, that depend on claims 1 and 10 respectively are allowable as are claims 1 and 10 and for the additional limitations recited therein.

The Examiner rejected claims 33, 37-42, 48-52 and 54 under 35 U.S.C. 103(a) as allegedly being obvious over Ramamurthy in view of Shinohara (U.S. Patent 6,122,251). The Examiner admits that Ramamurthy does not specifically disclose an ATM switch having output controls that monitor two or more data stores. However, the Examiner alleges that Shinohara (see FIG. 8) teaches a flow control system wherein an output control monitors the backlog of two or more data stores. The Examiner therefore alleges that it would have been obvious to one of skill in the art to combine the rate control method

taught by Shinohara with the switch of Ramamurthy. Applicant respectfully traverses this rejection.

Independent claims 33 and 42 recite an ATM switched comprised in part by "a plurality of output ports, each output port operatively associated with a plurality of data stores and an output control". Further as recited in independent claims 33 and 42 the output controls are "arranged to monitor the backlog of buffered data units buffered in two or more of said plurality of data stores". Applicant respectfully submits that the cited references alone or in combination do not disclose or suggest the claimed elements.

Ramamurthy does not disclose the monitoring of the backlog of buffered data units. Rather, referring to FIG. 9, Ramamurthy discloses a system having an output controller that simply monitors the level of a single output buffer and stops data flow when the buffer is full. Ramamurthy does not therefore, disclose or suggest the monitoring of the backlog of buffered data units stored in two or more of a plurality of data stores associated with a single output port. In fact in Ramamurthy the level of data stored in the plurality of input buffers is not monitored in any way by the controller of Ramamurthy.

In addition, referring to FIG. 8, Shinohara discloses a switch control circuit wherein a buffer occupancy measuring unit is used to measure the occupancy of a plurality of output buffers each of which is individually associated with a different output port. Shinohara simply allows a single output control to monitor the occupancy rate of each of the output ports rather than having an individual output control for each port. Shinohara does not however disclose or suggest an output control arranged to monitor the backlog of buffered data units in two or more data stores, each of which is operatively associated with the same output port. Therefore, the cited references do not disclose or suggest an output controller that monitors the backlog of buffered data units in two or more data stores, wherein

each of the two or more data stores are operatively associated with the same output port.

Accordingly, applicant respectfully submits that independent claims 33 and 42 recite a novel and unobvious apparatus in view of Ramamurthy and Shinohara and should therefore be allowed. Further claims 34-41 and claims 43-54, that depend on claim 33 and claim 42 respectively are allowable as are claims 33 and 42 and for the additional limitations recited therein.

Applicant's counsel conducted an interview with the Examiner on March 29, 2002. Applicant and the Examiner discussed the differences between Ramamurthy and the present invention. Applicant has amended the claims herein as discussed with the Examiner during the interview and respectfully requests issuance of a Notice of Allowance. In addition, during the interview, Applicant and the Examiner agreed that the Office action dated January 15, 2002 was incorrectly identified as a final rejection and that Applicant's amendment would be treated as a response to a non-final Office action.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (Twice Amended) An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections;

a plurality of output ports, each output port operatively associated with a plurality of output data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the output data stores on an output side of the switch fabric are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to monitor the backlog of buffered data units in one or more of said plurality of output data stores for delivery to their associated output ports and, if the backlog reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

10. (Twice Amended) An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections;

a plurality of output ports, each output port operatively associated with a plurality of output data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the output data stores on an output side of the switch fabric are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to monitor the backlog of buffered data units in one or more of said

plurality of output data stores for delivery to their associated output ports and, if the backlog buffered in one or more selected stores reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

33.(Amended) An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections;

a plurality of output ports, each output port operatively associated with a plurality of data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the data stores are arranged to buffer data units for delivery to their associated output ports, and the output controls are arranged to monitor the backlog of buffered data units buffered in two or more of said plurality of data stores for delivery to their associated output ports and, if the backlog reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

42.(Amended) An ATM switch, comprising:

a plurality of input ports for receiving data units on virtual connections;

a plurality of output ports, each output port operatively associated with a plurality of data stores and an output control; and

a switch fabric for switching data units from any of the input ports to any of the output ports;

wherein the data stores are arranged to buffer data units for delivery to their associated output ports, and the output controls are

arranged to monitor the backlog of buffered data units buffered in two or more of said plurality of data stores for delivery to their associated output ports and, if the backlog buffered in one or more selected stores reaches a particular level, to enforce a rate limitation against additional data units for delivery to their associated output ports, wherein the additional data units in violation of the rate limitation are filtered.

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